THE DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING SPEAKER SERIES

PRESENTS

There and Back Again: Leveraging Photonics for Designing Computing Systems

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LECTURE ABSTRACT

Today's computing systems primarily run data-centric applications such as machine learning, graph algorithms, and cognitive processing, which have large compute requirements and data footprints. Unfortunately, technology scaling has slowed down considerably and is not able to keep up with the growing compute and memory needs of these data-centric applications. We need to explore emerging technologies, and correspondingly new computing and memory architectures for these data-centric applications. In this talk, I'll talk about two of our ongoing projects on leveraging photonics for compute and memory.

On the compute front, I'll present the design of a hybrid electro-photonic accelerator called ADEPT. ADEPT leverages a photonic computing core for efficiently performing GEMM operations, a vectorized digital electronic ASIC for performing non-GEMM operations, and SRAM arrays for storing DNN parameters and activations. Different from prior art, we consider a complete hybrid system with photonic and non-photonic components, on-chip and off-chip data transfers, and communication cost. A head-to-head comparison of ADEPT with electronic systolic array architectures shows that ADEPT can provide, on average, 7.19× higher inference throughput per watt.

On the memory front, I'll present a unified network and main memory system called COSMOS that combines optically-controlled phase change memory (OPCM) and silicon-photonic links to achieve high memory throughput. COSMOS consists of a hierarchical multi-banked OPCM array with novel read and write access protocols. It uses an Electrical-Optical-Electrical (E-O-E) control unit to map standard DRAM

read/write commands (sent in electrical domain) from the memory controller on to optical signals that access the OPCM cells. COSMOS designed with state-of-the-art technology provides similar performance and energy as DDR5. Compared to an electrically controlled phase change memory system, our COSMOS system provides 2.09× higher read throughput and 2.15× higher write throughput, thereby reducing application execution time by 2.14×, read energy by 1.24×, and write energy by 4.06×.

SPEAKER BIOSKETCH

Dr. Ajay Joshi received his Ph.D. degree from Georgia Tech in 2006 and then worked as a postdoctoral researcher at MIT. In 2009, he joined the ECE department at Boston University, where he is currently a Professor and the Interim Associate Dean for Educational Initiatives. He was a Visiting Researcher at Google in 2017-18 and is currently an Architect at Lightmatter Inc. His research is in the areas of computer architecture and digital VLSI with current focus on security, machine learning and photonic computing. He received the NSF CAREER Award in 2012, Boston University ECE Department's Award for Excellence in Teaching in 2014, Best Paper Award at ASIACCS 2018, and Google Faculty Research Award in 2018 and 2019. He currently serves as the Associate Editor for IEEE Transactions on VLSI System.