

THE BIRTHING OF A MODERN INTEGRATED CIRCUIT TECHNOLOGY

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Few people who are not in the semiconductor industry appreciate the scale of the effort needed to develop and deploy a leading edge technology. In 2012 the state-of-the-art System on a Chip (SoC) technology with embedded flash EEPROM was at the 65nm technology node. This development project will be used as a case study to describe the steps undertaken to develop and qualify this technology. The architecture of two competing flash bitcells will be described along with the processes for reading, writing and erasing the cells. At that time the dominant technology was a stacked gate architecture sometimes referred to as FLOTOX or ETOX which is a type of charge storage device. In competition with this bitcell was another charge storage bitcell developed by Silicon Storage Technology of Sunnyvale CA known as Embedded Super Flash. It featured a split gate architecture. Both architectures had advantages and disadvantages which will be explained and the process for selecting one over the other will be examined. Included will be an example of cycling failures with the selected bitcell and how it was analyzed resulting in the discovery of a failure mechanism never seen before and therefore never checked. The key requirements for qualifying flash technology will be explained. The end result was a technology that delivered products to the safety, automotive, medical and internet-of-things (IOT) market. The Tiva-C SoC sometimes used by UH students was designed and manufactured in this technology. In addition to being made available to the catalog market, custom devices are being sold to Bosch, Continental-Teves, TRW, Visteon, AutoLiv, SiriusXM, and Apple among others.



Douglas Verret

Texas Instruments Inc., Retired

IEEE Life Fellow

SPEAKER BIO

Douglas Verret received an MS in physics from Purdue University, West Lafayette IN in 1974 and was an NSF Fellow. He received a PhD in Solid State Physics from the University of New Orleans, New Orleans LA in 1978 and was a Dana Fellow. He taught high school physics and math in New Orleans for five years and was an Instructor and Assistant Professor of Physics and Pre-Engineering at Xavier University, New Orleans LA for five years. In 1979 he joined Texas Instruments Inc in Stafford TX and served first as a process engineer and then as Bipolar and BiCMOS Development Manager. He retired from TI in 2014. During his thirty-five years at TI he lead the development of "glue" logic products built in bipolar and BiCMOS technologies and then FPGA products. The BiCMOS products were among the first in the industry. He is the principal inventor in sixteen US patents dealing with polysilicon emitters, deep trench isolation and Cu interconnects. He was elected TI Fellow in 1992. Dr Verret was CMOS Editor for the IEEE Transactions on Electron Devices from 1995-2000 and Editor-in-Chief from 2000-2011. He has been a member of the International Electron Devices Meeting Technical Committee as well as 1993 Technical Program Chairman of the Bipolar and BiCMOS Technology Meeting. He is a member of the Board of Governors of the Electron Devices Society (EDS) and was awarded the EDS Distinguished Service Award in 2012. He is also a member of the American Physical Society and Sigma Xi. He was elected IEEE Fellow in 2004. He is a past member of the Baylor University Department of Electrical and Computer Engineering Board of Advocates. He is currently Chairman of the UH ECE Department Board of Governors.

Contact Professor Jiming Bao at jbao@uh.edu if you would like to arrange for a time to meet with Dr. Verret.

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